disabling the integrated circuit if the input current exceeds the predetermined level.

REMARKS

1. A marked-up version of the rewritten claims is attached hereto.

2. Claims 2, 11, and 13 have been amended to make them definite, while claim 12 has been cancelled. It is therefore submitted that all claims conform to 35 U.S.C. 112, second paragraph.

The present invention is a power supply circuit and method which has both an inrush control and a power factor correction control. The invention features using a single control circuit to control both the inrush control circuit and the power factor correction circuit. This has the advantages of saving the cost and space of a second control circuit as well as not requiring synchronization between two control circuits.

Bernstein shows one drive circuit 38 and another drive circuit is required to connect to the gate of transistor 34.

Claim 1 recites that the active power factor correction circuit has a controller and an inrush current control circuit comprising a switch having a control element coupled to the controller. Claim 15 recites a controller controlling the power factor correct control circuit and an active current limiting device.

Since these features are not disclosed in Bernstein, the rejection of claims 1, 2, 4, 7, 8, 15, 16, 18, 19, 21 and 22 under 35 U.S.C. 102 on this reference should be withdrawn.

Further, since Bernstein does not suggest these features, the rejection of claims 3 and 17 under 35 U.S.C. 103 in view of Bernstein should be withdrawn.

Inn just shows an inrush protection circuit. Therefore combining it with Bernstein does not result in the present invention. Thus, the rejection of claims 5, 6, and 20 under 35 U.S.C. 103 on this combination should be withdrawn.

Nelson shows two control circuits 56 and 64. Claim 9 recites "…implementing the power factor control signal to actively control the inrush current…", i.e., the single control signal concept. Thus, the rejection of claims 9, 11 and 13 under 35 U.SC. 103 in view of Nelson should be withdrawn.

Since as discussed above, neither Nelson or Bernstein shows the present invention, the rejection of claims 10 and 14 under 35 U.S.C. 103 on this combination should be withdrawn.

For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record, and are in proper form for allowance. Accordingly, favorable reconsideration and allowance is respectfully requested. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

A check in the amount of $110.00 is enclosed for a one month extension of time and for additional claim fees. The Commissioner is hereby authorized to charge payment for any fees

associated with this communication or credit any over payment to Deposit Account No. 16-1350.

Respectfully submitted,

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March 12, 2002
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date indicated below as first class mail in an envelope addressed to the Commissioner of Patents, Washington, D.C. 20231.

Date: 3/12/02

Signature: Elaine F. Swan
Person Making Deposit

Application No.: 09/749,354

Marked Up Claim(s)

1. (Amended) A power supply circuit, the circuit comprising:

an active power factor correction circuit, the active power factor correction circuit having a controller; and

an inrush current control circuit, the inrush control circuit comprising at least one switch having a control element coupled [insulated gate bipolar transistor (IGBT) connectable] to the controller[, wherein each IGBT comprises a gate].

2. (Amended) A power supply circuit as in claim 1 wherein the switch [power circuit] comprises an IGBT [boost pre-regulator].

11. (Amended) A method as in claim 9 wherein the step of generating the power factor control signal further comprises the steps of:

charging at least one [integrated circuit (IC)] power capacitor to a predetermined voltage level; and

enabling at least one integrated circuit [on IC] associated with the at least one [IC power] capacitor.

13. (Amended) A method as in claim [12]11 wherein the step of enabling [the UC3854 IC drive output] further comprises the steps of:

determining an input current;

comparing the input current with a predetermined current level; and

disabling the integrated circuit [UC3854 IC] if the input current exceeds the predetermined level.